REMARKS

The present amendment is responsive to the official action mailed on March 30, 2001. The present amendment is also intended as a record of the telephonic interview between Examiner David Graybill and undersigned counsel on June 6, 2001. The Examiner's courtesy in conducting such interview are appreciated.

Claims 1-17 were rejected for double patenting under 35 U.S.C. § 101 "as claiming the same invention" as certain claims in prior U.S. Patent 5,950,070. As pointed out in the interview, however, the double patenting rejection under § 101 is believed to be legally inapplicable in the present situation. As noted in the official action itself, the § 101 double patenting rejection is grounded in the language of § 101 which provides that an inventor may obtain "a patent", i.e., that a particular inventor may obtain only one patent for the identical invention. The entire doctrine of double patenting, including statutory double patenting under § 101, relates to multiple applications and/or patents of a common invented entity or common owner. "Before consideration can be given to the issue of double patenting, there must be some common relationship of the inventorship and/or ownership of two or more patents or applications." MPEP 804.

U.S. Patent, 5,950,070 is not owned by the present assignee and the named inventors in the '070 patent are not the same as the named inventors in the present application. Stated another way, the '070 patent named inventors and the present named inventors are adverse parties. Both are claiming the same invention. In that situation, 35 U.S.C. § 135 requires that the Patent and Trademark Office determine priority of invention by an interference proceeding. Indeed, Chart IIA incorporated in MPEP 804 expressly provides that where an application and patent contain conflicting claims to the same invention and there is no common assignee or inventor, the Examiner is to suggest claims

for interference.[1] In the telephone interview, the Examiner indicated that, subject to further reconsideration, it did appear that the § 101 double patenting rejection was inapplicable. Accordingly, such rejection should be withdrawn and an interference between the present application and the '070 patent should be declared.

Claims 1-17 were rejected under 35 U.S.C. § 112, second paragraph as indefinite. As pointed out in the interview however, present claims 1-6 are exact copies of claims 1, 2, 6, 7, 8 and 10, respectively in the '070 patent. The § 112, second paragraph rejections of these claims manifestly would be applicable to the identically worded claims of the '070 patent. The rejections of present claims 7-17 are based on exactly same alleged defects and also would be applicable to the claims in the '070 patent. The office should not apply § 112, second paragraph to applicant's claims with a greater degree of strictness than was applied in examination of the '070 claims. Such disparate treatment could unfairly impact on applicant's right to contest priority of invention. To avoid such disparate treatment, Office policy provides that any rejection of a claim which would also be applicable to a corresponding patent claim must be approved by the group director. MPEP 2307.02. Based upon the Official Action, it does not appear that such approval was obtained in the present case. Accordingly, it is respectfully requested that the § 112, second paragraph rejection be reconsidered.

As discussed in the interview, however, in the interest of advancing prosecution, applicant has presented new claims 18-34. These claims are verbatim identical to claims 1-17 respectively, except that the new claims have been rephrased to correct the deficiencies noted in the § 112, second paragraph

[1] The other possibility suggested in the Chart -- applying a rejection in the application under § 102(e) based on the patent -- is manifestly inapplicable here. The present application has an effective filing date many years prior to the alleged effective filing date of the '070 patent.

rejection. Although the new claims are not technically amended claims which would require presentation of a marked copy to show the changes in the claims, such a marked copy is provided as Exhibit A to the present amendment to facilitate review. This Exhibit shows the differences between claims 18-34 and original claims 1-17. The amendatory matter is believed to be self-explanatory. Further, it is respectfully submitted that the differences between original claims 1-17 and new claims 18-34 do not change the invention set forth therein and said new claims 18-34 continue to claim the same invention as claims in the '070 patent. It is also respectfully submitted that the new claims are free of the deficiencies noted in the Official Action.

Claims 6, 12 and 17 were rejected under 35 U.S.C. § 112, first paragraph as containing subject matter not described in the specification. The "amendment filed September 7, 2000" was objected to under 35 U.S.C. § 132 as assertedly introducing new matter into the disclosure. The basis for this objection was the same as the § 112, first paragraph rejections. It is respectfully submitted that claims 6, 12 and 17 and claims 23, 29 and 34 directed to the same subject matter are fully supported by the specification. See FIG. 13 and the related text of the present specification. At page 33, lines 9-10, the "interposer 836" (referred to in the patent claims as a "section of a dielectric interposer") is referred to as having "edges 846". In the text at page 34, lines 9-37, the wire bonding operation is described. It is expressly stated that the composite lead formed by the wire bonding operation "extends across the edge 846 above the interposer." The drawing and text make it plain that the bonding wires extend across the edges. FIG. 13 shows one bonding wire 856 (at the lower left hand corner of the drawing) extending at an angle to edge 846 different from the angles between the other bonding wires and the same edge. Manifestly, at least one bonding wire extends at an angle other than 90° to the particular

edge 846 seen in the fragmentary of FIG. 13. The same interposer 836 is also illustrated in full plan view in FIG. 12. It is apparent that the interposer 836 is rectangular and hence the various edges 846 of the interposer lie at right angles to one another. A bonding wire which extends at an angle of other than 90° to the single edge depicted in FIG. 13 is also at an angle of other than 90° to any edge of the interposer or "section", as recited in new claims 23, 29 and 34, and as recited, in different phraseology, in claims 7, 12 and 17. Accordingly, § 112 rejection and the related objections should be withdrawn.

It is respectfully requested that the present claims be held allowable to applicant. As it is believed that all of the objections, rejections and requirements set forth in the Official Action has been fully met, favorable reconsideration and declaration of an interference between the present application and the '070 patent are earnestly solicited.

Respectfully submitted,

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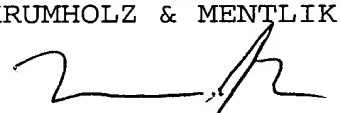

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EXHIBIT A

New Claims Showing Differences Vis-à-vis Claims 1-17

18. A method of assembling a plurality of semiconductor chips, comprising the steps of:

(a) providing a portion of a semiconductor wafer containing the plurality of chips thereon, each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;

(b) assembling a respective section of a dielectric interposer to each respective one of the plurality of chips individually, without detaching the plurality of chips from the portion of the semiconductor wafer, each section of interposer having a plurality of bonding pads near an outer periphery of the section, such that each bonding pad lies near the contact pattern area of the corresponding one of the plurality of chips;

(c) wire bonding each bonding pad to a respective one of the contacts on the front surface of the corresponding one of the plurality of chip whereby wires extend from the bonding pads to the contacts;

(d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and

(e) cutting the encapsulated chips from the semiconductor wafer.

19. A method according to claim 18, wherein step (c) includes bonding one end of each one of said wires to a respective bonding pad using one of the group consisting of micro resistant welding and ultrasonic bonding.

20. A method according to claim 18, wherein step (b) includes providing an elastomer between each of the plurality of chips and the respective interposer on the chip.

21. A method according to claim 18, wherein the portion of the semiconductor wafer includes the whole semiconductor wafer.

22. A method according to claim 18, wherein one end of each wire is bonded to a respective bonding pad of the interposer using ultrasonic bonding, and the other end of each wire is bonded to a respective contact of the chip using ultrasonic bonding.

23. A method according to claim 18, wherein each said section of the interposer has edges and wherein step (c) includes bonding one of the wires extending from a bonding pad of one said section so that said one of the wires ~~that~~ is oriented at an angle ~~substantially less~~ other than 90 degrees from any edge ~~side~~ of ~~the~~ said one said section ~~of interposer having the bonding pad to which the one wire is bonded~~.

24. A method of assembling a plurality of semiconductor chips, comprising the steps of:

(a) providing a portion of a semiconductor wafer containing the plurality of chips thereon, each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;

(b) assembling a sheet including a plurality of interposers to said portion of said semiconductor wafer so that each said interposer is assembled to an associated one of the plurality of chips, without

detaching the plurality of chips from the portion of the semiconductor wafer, each said interposer having a plurality of bonding terminals near an outer periphery of the interposer, such that each bonding terminal of each said interposer lies near the contacts of the one of the plurality of chips associated with that interposer;

(c) wire bonding each bonding terminal to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips whereby wires extend from the bonding pads to the contacts;

(d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and

(e) cutting the encapsulated chips from the semiconductor wafer.

25. A method according to claim 24, wherein step (c) includes bonding one end of each one of said wires to a respective bonding terminal using ultrasonic bonding.

26. A method according to claim 24, wherein step (b) includes providing an elastomer between each of the plurality of chips and the interposer associated with that chip.

27. A method according to claim 24, wherein the portion of the semiconductor wafer includes the whole semiconductor wafer.

28. A method according to claim 24, wherein one end of each wire is bonded to a respective bonding terminal of the interposer using ultrasonic bonding, and

the other end of each wire is bonded to a respective contact of the chip using ultrasonic bonding.

29. A method according to claim 24, wherein each said section of the interposer has edges and wherein step (c) includes bonding one of the wires extending from a bonding pad of one said section so that said one of the wires ~~that~~ is oriented at an angle ~~substantially less~~ other than 90 degrees from any ~~side~~ edge of ~~the~~ said one said section ~~of interposer having the bonding terminal to which the one wire is bonded~~.

30. A method of assembling a plurality of semiconductor chips, comprising the steps of:

(a) providing a semiconductor wafer containing the plurality of chips thereon, each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;

(b) assembling a sheet including a plurality of interposers to said semiconductor wafer so that each said interposer is assembled to an associated one of the plurality of chips, without detaching the plurality of chips from the semiconductor wafer, each said interposer having a plurality of bonding terminals near an outer periphery of the interposer, such that each bonding terminal of each said interposer lies near the contacts of the one of the plurality of chips associated with that interposer;

(c) wire bonding each bonding terminal to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips whereby wires extend from the bonding pads to the contacts;

(d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and

(e) cutting the encapsulated chips from the semiconductor wafer.

31. A method according to claim 30, wherein step (c) includes bonding one end of each one of said wires to a respective bonding terminal using ultrasonic bonding.

32. A method according to claim 30, wherein step (b) includes providing an elastomer between each of the plurality of chips and the interposer associated with that chip.

33. A method according to claim 30, wherein one end of each wire is bonded to a respective bonding terminal of the interpose using ultrasonic bonding, and the other end of each wire is bonded to a respective contact of the chip using ultrasonic bonding.

34. A method according to claim 30, wherein each said section of the interposer has edges and wherein step (c) includes bonding one of the wires extending from a bonding pad of one said section so that said one of the wires~~that~~ is oriented at an angle ~~substantially less~~ other than 90 degrees from any ~~side~~ edge of ~~the~~ said one said section ~~of interposer having the bonding terminal to which the one wire is bonded~~.